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Design and Comparative Analysis of CNTFET based Tristate Buffer for Multiplexer

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ABSTRACT: Circuit designing has traditionally been amalgamated with CMOS model. However increasing demand of portable electronics and the need to lower the power consumption has led to expeditious progress in low power VLSI design. With the advent of modern CNTFET based technology, customary silicon based CMOS devices are being replaced. The present paper attempts to analyse the performance of CNT based Tristate Buffer and further design a 2X1 Multiplexer (MUX) using the designed CNT Tristate Buffer. Design and simulation of CNT based Tristate Buffer and 2X1 MUX is compared with their conventional MOS counterparts using HSPICE and the analysis has been performed at 45 nm technology node. It is thereby concluded from the results that CNT based Tri State Buffer and Multiplexer are faster, more accurate and less power consuming than conventional MOS Tri State Buffer and Multiplexer.

Keywords: CMOS, CNT, CNTFET, Tristate Buffer, MUX, simulation

I. INTRODUCTION

Throughout the past few decades, the semiconductor engineering has witnessed enormous performance developments and shrivelling in device geometries. The potential of VLSI circuits lies in more and more channel length reduction but existing fabrication technologies disallow further decrease in it. This is because of various short channel effects that arise in MOSFET like Drain-induced barrier lowering and punch-through, Surface scattering, Velocity saturation, Impact ionization and Hot electrons. The intrinsic gain of the transistor becomes low because of the inferiority in the device output impedance [1]. Therefore, Nano-Electronic device such as CNTFET (Carbon Nano Tube Field Effect Transistor) serve as a substitute for traditional CMOS technology. But the increased speed of operation (due to increase in clock speed) and very high number of transistors on a single chip (due to shrink in individual transistor size) lead to large power dissipation in MOSFET based devices [2]. This further causes more heat generation and therefore additional cost for heat removal. Also it is to mention that most of the devices used nowadays are portable which run on battery and their battery life is limited. The battery technology is not advancing at the same speed as VLSI, hence formulating power management as a substantial concern of contemporary times. This paper aims to demonstrate with the help of results, how CNTFET aids in overcoming the performance related issues of MOSFET and thus paves way to greater knowledge and more intensive research. This is done by comparing the results of CNTFET based Tristate Buffer and Multiplexer with the conventional MOSFET based equivalents.

This paper consist of 6 sections which includes the introductory part. A brief introduction is given on tristate buffer and multiplexer in section A and B respectively. Section II gives a brief explanation on CNTs and CNTFETs. All the circuit diagrams used in the designing of the devices are illustrated in section III. The simulation results obtained from these circuits are described in section IV. The conclusion of the paper is given in section V. Lastly, the challenges faced are explained in section VI.

A. Tristate Buffer

A Tristate Gate is a digital circuit that exhibits three states. Two of the states are signals, equivalent to logic 1 and logic 0 as in a conventional gate representing input and output. The third state is High Impedance (Z) state which behaves like an open circuit, this means that the output is disconnected and does not have any logic significance [3].

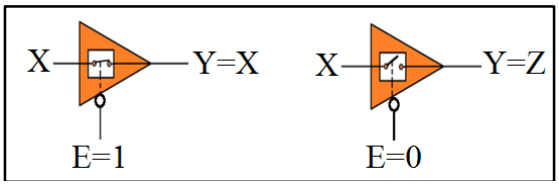

Fig. 1. Tristate Buffer Switch Equivalent (for active-low).

Enable input(E) determines the output state. When E=0, output is enabled and the gate behaves like any conventional buffer, with the output(Y) equal to the input(X), i.e. Y=X. When E=1, output is disabled and the gate goes to a high-impedance state(Z), regardless of the value in the normal input. Therefore making Y=Z. These conditions are applicable only for active-low buffers.

Tristate buffers can be of four types as explained below:

Active-High Tri-State Buffer: When Enable is 1, output is equal to input. When Enable is 0, output is equal to high impedance state.

Active-High Inverting Tri-State Buffer: When Enable is 1, output=inverted input. When Enable is 0, output is equal to high impedance state.

Table 1: Truth Table for Tristate Buffer (for active low).

Input	Enable	Output
0	1	Z (High Impedance)
1	1	Z (High Impedance)
0	0	0
1	0	1

Active-Low Tri-State Buffer: When Enable is 0, output=input. When Enable is 1, output is equal to high impedance state.
Active-Low Inverting Tri-State Buffer: When Enable=0, output=inverted input. When Enable is 1, output is equal to high impedance state.
Tristate Buffers find their use in a lot of applications. They can be used for designing the common bus system, for connecting multiple devices on a single communication bus as an output stage, and configured as open-drain or push-pull to support high fan-out to eliminate cross talk caused due to inter electrode capacitance due to close routing.

B. Multiplexer

It is a combinational circuit which is used to select one of the many inputs given and place them on the output line at different times. It consist of input lines, select line and one output line. The select line is used to select one the many inputs given and transfer it to the output. This type of multiplexing is referred as Time Division Multiplexing [4]. If a multiplexer (MUX) consist of 'n' select lines then it should have 2^n input lines. Example – A 2X1 MUX has two input, one select and one output line. A 2X1 MUX can also be considered as 'switch logic'. Multiplexer are also known as Data n selector, parallel to serial converter, many to one circuit and universal logic circuit. These are mainly used for increasing the amount data which is sent over a network with certain amount of time or bandwidth. Multiplexers can also be used as programmable logic devices. A logic circuit can be designed by defining a logic arrangement of input signals [5].
A simplified diagram of 2X1 MUX is shown below:

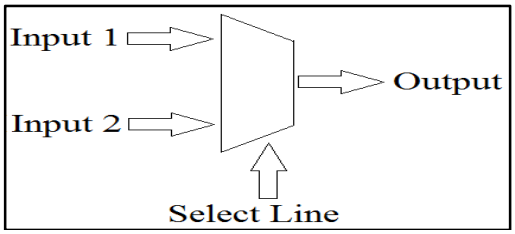

Fig. 2. 2X1 MUX.

If select line is at logic 1 then the signal at Input 2 will be transferred to the output. If select line is at logic 0 then the signal at Input 1 will be transferred to the output.

II. CNT AND CNTFET

As the size of the silicon MOSFET devices is being reduced, they are meeting various challenges. Therefore new materials are being tried and tested for new results and advancements. One of these is Carbon Nano Tubes (CNTs) which are being studied a lot in recent years in semiconductor industry [6][7]. Carbon nanotubes (CNTs) belong to type of Nanomaterial that are made up of two dimensional lattice of carbon atoms hexagonally attached and joined to form empty cylinder in one direction.

Table 2: Truth table for 2X1 MUX.

Input 1	Input 2	Select Line	Output
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	1
0	0	0	0
0	1	0	0
1	0	0	1
1	1	0	1

Carbon nanotubes belong to the fullerene class of carbon allotropes. There are numerous applications of CNTs in nanotech industry, optical industry and other areas of material science, also includes architectural areas where it show its potential [8][9].
These exhibit massive strength and unique electrical and conductive properties [1]. CNTs are very good conductors of heat because of carbon-carbon covalent bond, where the atomic radii of carbon atom and the free electrons are available in graphite like configuration. Other properties and performances include short channel effects, high normalised drive currents and high mobility.
CNTs with cylindrical structure could be either single-wall CNT (SWCNT) or multi-wall CNT (MWCNT). Depending on the chirality vector (n1, n2) a single wall CNT can be either semiconducting or metallic. Chirality vector specifies the arrangement of carbon atoms along the nanotube. If the value of n1-n2 is not a multiple of 3 then a single wall CNT is either semiconducting or metallic [10-11].
CNTFETs are advantageous over MOSFET as they have very less power dissipation and propagation delay. They also have improved control over channel formation, better threshold voltage, enhanced sub-threshold slope, high current density, high transconductance and high linearity. Due to high dielectric material, mobility of carrier increases whereas channel dimension decreases rigorously. The on/off currentis comparatively high. CNTFETs allow a better frequency curve at a gain twice that of MOSFETs.
Since the size of CMOS circuits is decreasing aggressively, it has led to higher integration density and more complexity in functionality. Sizing the MOSFET so small, below tens of nanometre leads to low transconductance, low ON current, leakage in gate oxide, decreasing mobility and enhanced delay. CNTFETs are suitable devices that have potential to keep up with smaller size and improving its performance at the same time [12-14]. Diagram below represents SWCNT, MWCNT and schematic of CNTFET.
The working of Carbon Nanotube Field Effect Transistor is analogous to that of a Metal Oxide Semiconductor Field Effect Transistor. The turning ON/OFF of the device is dependent on the gate voltage. This is capacitively coupled with the channel [15].
A single CNT or multiple CNTs in form of an array are used in to make CNTFET where silicon bulk in usual MOSFET is replaced with CNT as the channel material which results in increased density of drive current, because of large mobility of carriers in CNTS in comparison with traditional MOSFET bulk silicon [16].

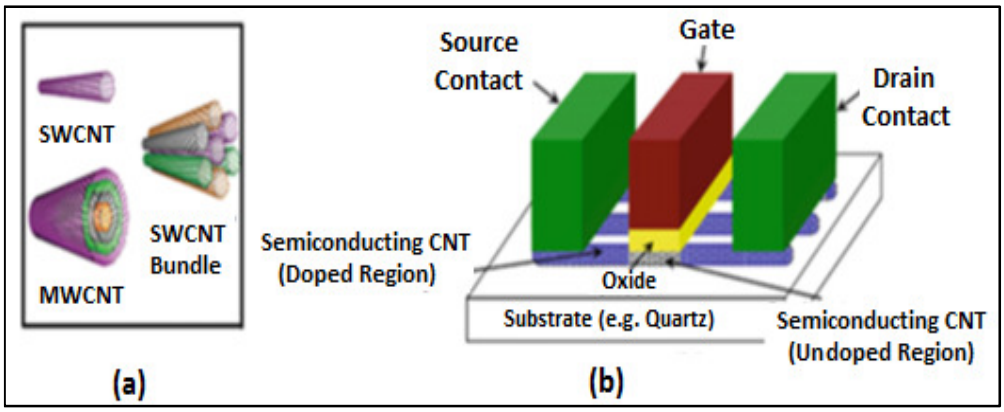

Fig. 3. (a) SWCNT and MWCNT (b) Schematic of a CNTFET.

From figure 1, it can be seen that the un-doped segments of CNT act as a channel under the gate electrode. While CNT which are heavily doped offer low electrical resistance when CNTFET is in ON state [17]. Gate width can be approximated as follows [18-19]:

$$W = \min (W_{min}, N \times S) \quad (1)$$

Where W_{min} is defined as the minimum value if gate width, N refers to number of tubes and S is the pitch value. Pitch is defined as the distance between two adjoining tubes. Threshold voltage of CNTFET can be controlled by the diameter of CNT. It can be approximated in terms of half band gap and is calculate from the formula as shown below:

$$V_{th} = \frac{E_g}{2e} = \frac{aV_\pi}{\sqrt{3}eD_{CNT}} = \frac{0.436}{D_{CNT}} \quad (2)$$

Where a (=0.249 nm) is the distance between two carbon atoms, e is the electron charge and V_π is carbon π- π bond energy in tight bonding model. D_{CNT} is the diameter of CNT and can be calculated as [18]:

$$D_{CNT} = \frac{a}{\pi}\left(\sqrt{n1^2 + n2^2 + n1n2}\right) \quad (3)$$

Where n1, n2 are the chirality vectors. Thus chirality vector is also a factor for threshold voltage.

III. CIRCUIT DIAGRAMS

A. Conventional CMOS based Circuit Diagrams

A Tri State Buffer designed using CMOS comprises of 8 MOSFETs (4 PMOS and 4 NMOS). The circuit can be explained in three sections. The first section, consisting of a PMOS (M1) and a NMOS (M2) form an inverter. Enable signal is given as input to the first section and also to the PMOS (M6) of the second stage. The output of the first section, i.e. NOT (Enable) is fed as input to the NMOS (M3) of the second section. The input signal is applied to M4 andM5. The third section is again an inverter (M7 and M8) to obtain the non-inverted output. All connections are as shown in the diagram above.

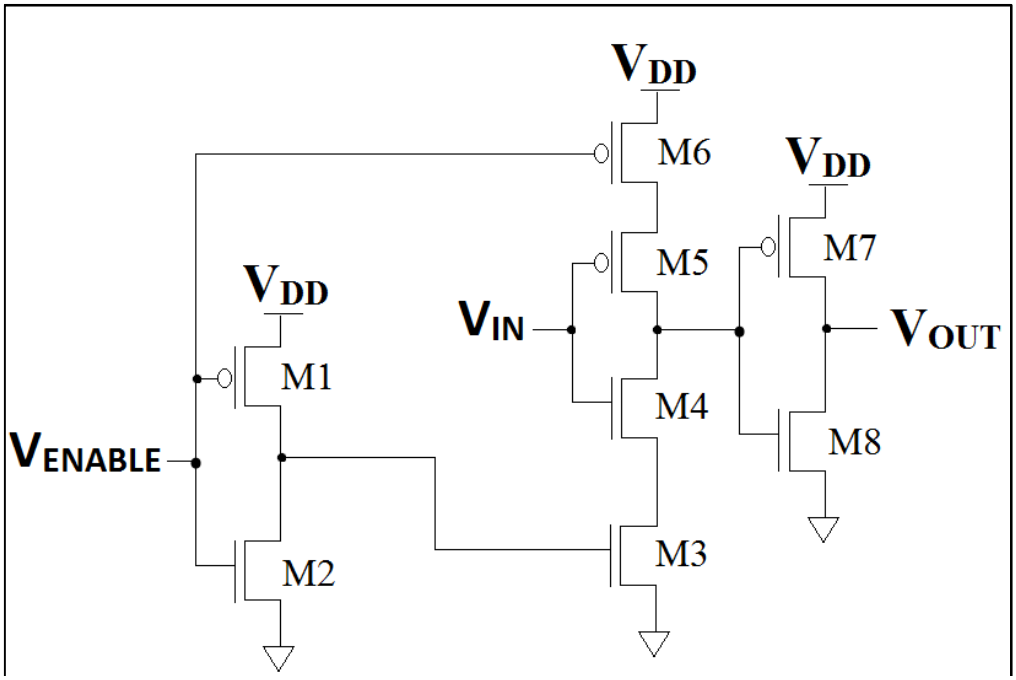

Fig. 4. CMOS based Tristate Buffer (for active low).

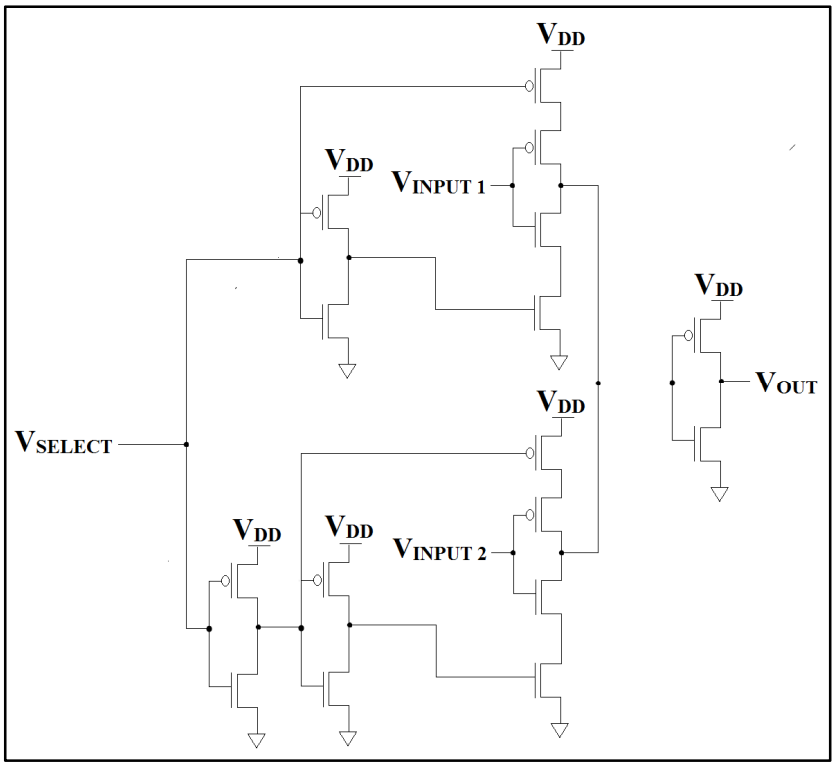

Fig. 5. CMOS based 2X1 MUX using tristate buffer.

A 2X1 MUX designed using tristate buffers comprises of 2 inverting tristate buffers and 2 inverters as shown in the above diagram. Two input signals (V_{INPUT1} and $V_{INPUT 2}$) are given at the input terminal and the required signal is obtained at the output (V_{OUT}). The upper section with V_{INPUT1} determines the first tristate buffer and the lower section with V_{INPUT2} determines the second tristate buffer. Select line (V_{SELECT}) is directly connected to first tristate buffer, whereas Select line (V_{SELECT}) is connected through an inverter to second tristate buffer. Output of both inverting tristate buffers is then finally connected to an inverter to obtain a non-inverting output. All connections are as shown in the diagram above.

Working: When V_{SELECT} is at logic 1, then V_{INPUT2} is obtained at V_{OUT}. When V_{SELECT} is at logic 0, then V_{INPUT1} is obtained at V_{OUT}.

B. Circuits designed using CNTFET

The design of CNTFET can be modelled on the design of MOSFET as explained earlier.

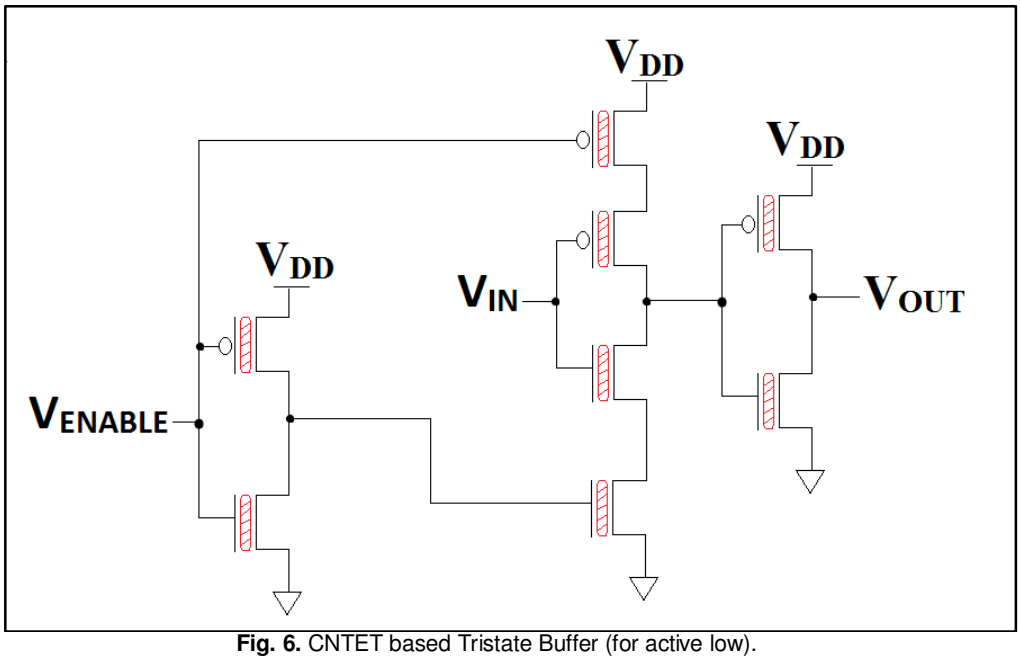

Fig. 6. CNTET based Tristate Buffer (for active low).

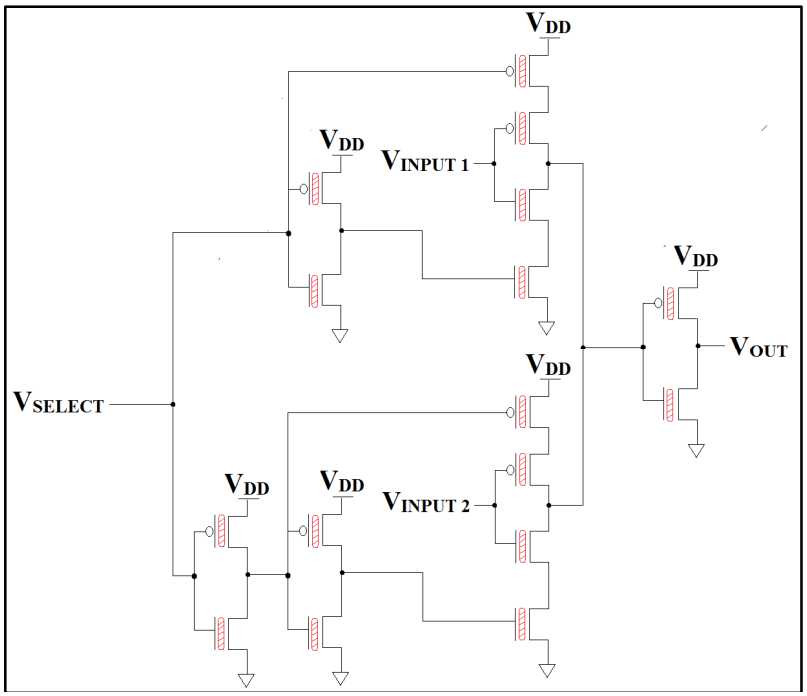

Fig. 7. CNTFET based 2X1 MUX using tristate buffer.

The design of CNTFET can be modelled on the design of MOSFET as explained earlier.

IV. SIMULATION RESULTS

A. CMOS based Circuits: Simulation Results

A tristate buffer output can be analysed from the above graph. It is seen that CMOS based buffer contains spikes and glitches.

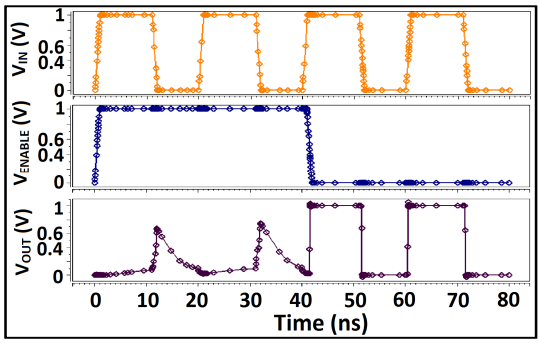

Fig. 8. CMOS based Tristate Buffer output.

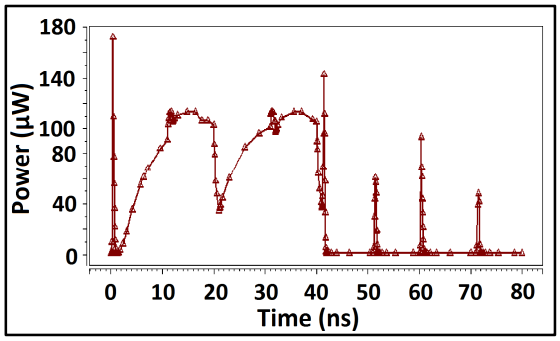

Fig. 9. CMOS based Tristate Buffer Power Plot.

Average power of CMOS based tristate buffer was found to be 4.5090E-05 Watts from 2.0000E-10 to 8.0000E-08 seconds. It consumes more power for a large time period.

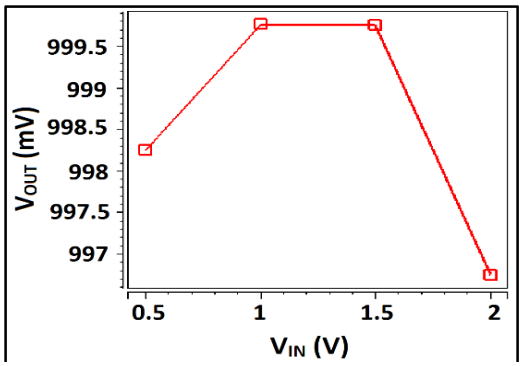

Fig. 10. DC response of CMOS based Tristate Buffer.

From the DC response of CMOS based Tristate Buffer, it can be seen that the maximum output voltage (V_{OUT}) is 999.8 mV at an input voltage (V_{IN}) of 1 V to 1.5 V.

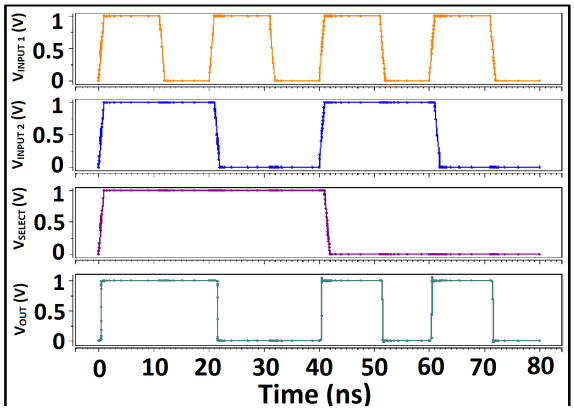

Fig. 11. CMOS based 2X1 MUX using Tristate Buffer output.

The minimum output voltage (V_{OUT}) is 996.7 mV at an input voltage (V_{IN}) of 2 V. Hence, it can be seen, if the input voltage is accidentally increased (from 1.5 V to 2 V) then there will be a decrease in the output voltage. This shall result in abnormal operation.

A 2X1 MUX using tristate buffer can be analysed from the above graph. It is seen that CMOS based buffer contains spikes and glitches especially when the output wave rises to 1V. It has less resemblance with input waveforms.

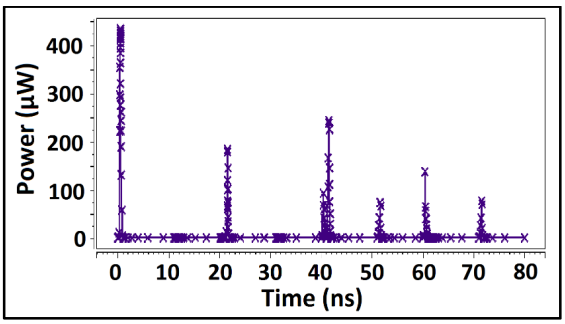

Fig. 12. CMOS based 2X1 MUX Power Plot.

Average power of CMOS based 2X1 MUX was found to be 6.2798E-06Watts from 2.0000E-10 to 8.0000E-08 seconds. The maximum power consumed is approximately equal to 450 micro-watts as seen from the graph.

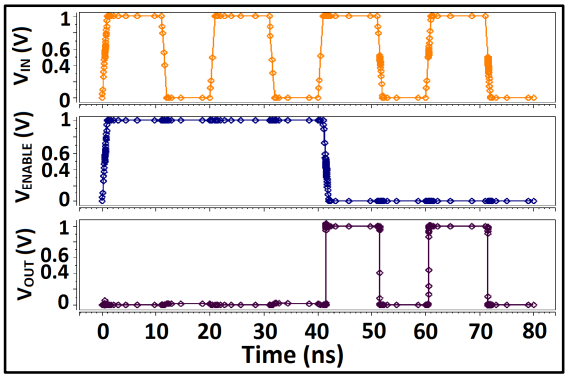

Fig. 13. CNTFET based Tristate Buffer Output.

It is seen that CNTFET based buffer contains comparatively less spikes and glitches. Hence, resembles more to the input waveform.

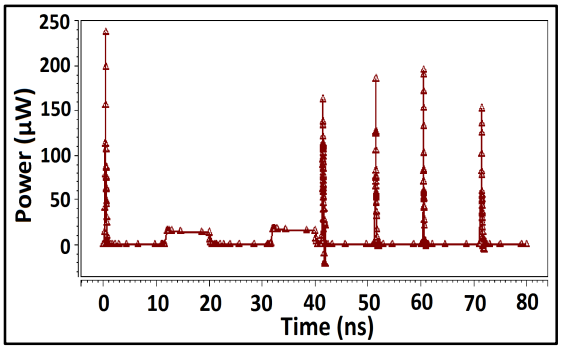

Fig. 14. CNTFET based Tristate Buffer Power Plot.

Average power of CNTFET based tristate buffer was found to be 4.8862E-06 Watts from 2.0000E-10 to 8.0000E-08 seconds. In comparison to CMOS based tristate buffer, CNTFET based tristate buffer consumes very less power and that too for a small time period.

B. CNTFET based Circuits: Simulation Results

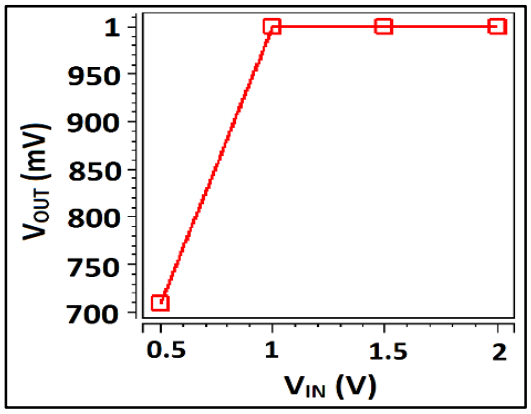

Fig. 15. DC Response of CNTFET based Tristate Buffer.

From the DC response of CNTFET based Tristate Buffer, it can be seen that the maximum output voltage (V_{OUT}) is 1.0 V at an input voltage (V_{IN}) of 1 V to 2 V. The minimum output voltage (V_{OUT}) is 710 mV at an input voltage (V_{IN}) of 0.5 V. Hence, it can be seen, if the input voltage is accidentally increased (from 1 V to 2 V) then even the device will continue to perform normally.

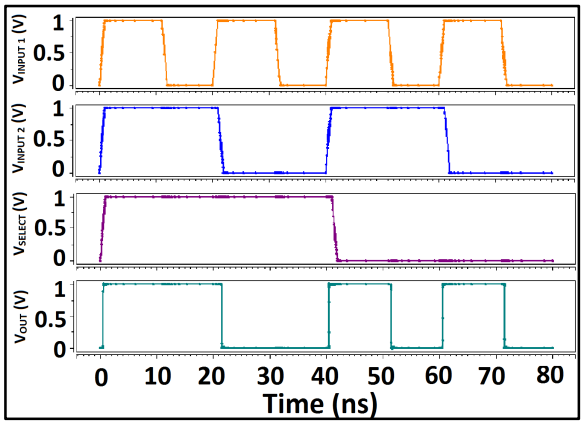

Fig. 16. CNTFET based 2X1 MUX using Tristate Buffer output.

A 2X1 MUX using tristate buffer output can be analysed from the above graph. It is seen that CNTFET based buffer contains very less spikes and glitches. It has much more resemblance with input waveforms as compared to CMOS based 2X1 MUX.

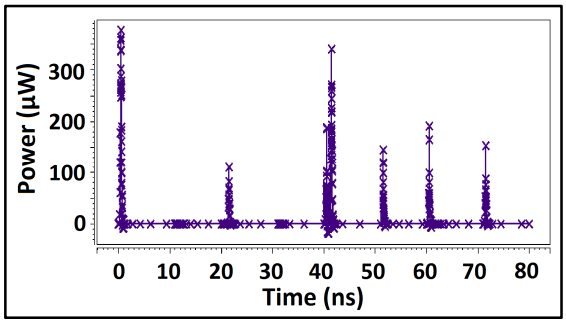

Fig. 17. CNTFET based 2X1 MUX Power Plot.

Average power of CNTFET based 2X1 MUX was found to be 3.0290E-06Watts from 2.0000E-10 to 8.0000E-08 seconds. The maximum power consumed is approximately equal to 380 micro-watts as seen from the graph.

Parameters used in designing of the circuits:

Design parameters for MOSFET based Tristate buffer and 2X1 MUX used are: V_{DD} = 1 V, Width of Channels = 381.5 nm. This was simulated using BSIMv4.6.1 Berkeley Predictive Technology model at the 45 nm technology node for MOSFETs.

Proposed CNTFET based Tristate Buffer and 2X1 MUX are simulated using Stanford CNFET model with V_{DD} = 1 V, Width of Channels = 381.5 nm, Number of CNTs (N) = 20, Pitch (S) = 20 nm, Diameter of CNT (D_{CNT})=1.5 nm. Other parameters for CNTFET based devices are shown below:

Table 3: CNTFET device parameters used in the proposed CNT based Tristate Buffer.

Device Parameter	Description	Default value
Lch	Physical channel length	45.0nm
Lgeff	MFP in the intrinsic CNT channel	200.0nm
Lss	Doped CNT source-side extension length	32.0nm
Ldd	Doped CNT drain-side extension Length	32.0nm
Efi	Fermi level of doped S/D tube	0.6eV
Kgate	Dielectric constant of high-k top gate	16.0
Tox	Thickness of high-k top gate	4.0nm
Csub	Coupling capacitance between channel and the substrate	20.0pF/m

V. CONCLUSION

As the technology scaling continues, many design methodologies have to be employed in order to uphold the VLSI trend. Owing to several scaling effects, the performance of CMOS gets influenced. To improve the performance characteristics, CNT is studied and evaluated. The key contribution of this paper is to be able to design and simulate CNT based Tristate Buffer and a 2X1 Multiplexer using that Tristate Buffer. The graph of Tristate buffer and 2X1 MUX obtained from the simulations illustrate that as compared to MOSFET, in CNTFET: the edges of waveform are sharper and contain less glitches. The output resembles the input to a large extent, hence CNTFET based Tristate buffer and 2X1 MUX is more accurate than MOSFET based Tristate buffer and 2X1 MUX. It is also found that there is less power consumption in CNTFET which improves its performance. Therefore, CNT technology is significantly better weighed against CMOS technology. Its performance can be further improved by using optimized values of CNT parameters. In future, the study can be extended by physically investigating the circuits and observing its performance. It will corroborate our study to an industrial basis.

VI. CHALLENGES

To keep up with the exceptional intensification of VLSI, enhancement is required on all ends. The inadequacy of fabrication (technology, capital and time) proves to be the principal hurdle that is hindering the expansion of the CNT industry. Scaling, high frequency of operation and low power voltages contribute to the destructive impact on reliability. Collectively, they add to the amount of discontinuities and transient errors. Extraordinary speed designing with gate count of millions, clock allocation, time to market, reuse, portability and predictability are the other challenges that are threatening CNT industries. There are no CNTFETs in the market as it is very tough to produce a reliable, defect free, economical fabrication process for CNT. Also, there are limited modelling resources for simulating CNT properties in bulk form. Recuperating the electrical and mechanical properties of bulk CNT to more closely resemble individual CNT will facilitate a colossal influence on industries. There is at all times a necessity to have energy proficient circuits for lower power consumption with escalating density of transistors. In the long run, CNTs will substitute silicon and even the most fundamental technology will have it as an essential constituent.

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